adjacent a silicon dioxide region, (d) the conductor comprises one or more of titanium tungsten, platinum silicide, aluminum and aluminum alloy, (e) the body region of the device comprises a heavily doped contact region, and (f) the device comprises a p-type region that is below the Schottky diode and in contact with the perimeter of the Schottky diode.

[0010] In some embodiments, at least some of the said MOSFET cells and at least some of the Schottky diode cells are arranged in a geometric configuration that is selected from an in-line square geometry, an offset square geometry, and a hexagonal geometry.

[0011] In other embodiments, at least some of the MOSFET cells are octagonal cells. For example, at least some of the MOSFET cells and at least some of the Schottky diode cells can be arranged in a geometry that comprises alternating first and second cell rows, in which the cells of the first cell rows are greater in area than the cells of the second cell rows, and in which the cells of the first cell rows are octagonal cells. The octagonal cells can be, for example, regular octagons. The MOSFET cells can be positioned, for example, in the first cell rows, and the Schottky diode cells can be positioned, for example, within the second cell rows. Cells of the second cell rows can include, for example, octagonal cells or square cells.

[0012] According to another embodiment of the invention, a merged device is provided that comprises Schottky diode cells and MOSFET cells. In this embodiment, the Schottky diode cells are located at the bottom of a trench network, while certain gate regions of the MOSFET cells are provided on sidewalls of the trench network.

[0013] According to another embodiment of the invention, a method of forming a merged device is provided. The method comprises forming a plurality of Schottky diode cells and forming a plurality of MOSFET cells, such that: (a) the Schottky diode cells are located at the bottom of a trench network, (b) the gate regions of the MOSFET cells comprise a conductive region and an insulating region, (c) certain of the gate regions are provided on sidewalls of the trench network, and (d) the conductive regions of the gate regions are formed without the aid of a masking layer, preferably by etching a doped polysilicon layer using an anisotropic etching process.

[0014] According to another embodiment of the invention, a method for designing a merged device, which comprises a plurality of Schottky diode cells and a plurality of MOSFET cells, is provided. The method comprises: (1) removing one or more source/body mesas within a trench MOSFET device design and (2) locating one or more Schottky diode cells where the removed mesa was formerly located.

[0015] One advantage of the present invention is that a merged device is provided that contains both a DMOS transistor and a Schottky diode integrated on the same substrate.

[0016] Another advantage of the present invention is that the DMOS transistor and Schottky diode portions of the merged device can be created in an integrated manufacturing process, rather than being created sequentially.

[0017] Another advantage of the present invention is that a merged device is provided that optimizes surface area utilization by incorporating DMOS transistor function into the sidewalls of the trenches that are used to provide the Schottky diode function of the device.

[0018] Another advantage of the present invention is that the geometry of the device can be selected to vary the ratio of DMOS source perimeter to Schottky diode conducting area, optimizing device performance.

[0019] Yet another advantage of the present invention is that the ratio of DMOS source perimeter to Schottky-diode conducting area can be varied across the device, optimizing device performance at edges and as a function of temperature.

[0020] Still other embodiments and advantages of the present invention will become readily apparent to those skilled in the art upon review of the Detailed Description, Examples and Claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] **FIG. 1** shows a schematic cross-sectional view of a vertical power MOSFET of the prior art.

[0022] **FIG. 2** shows a schematic cross-sectional view of a trench power MOSFET of the prior art.

[0023] **FIG. 3** is a schematic circuit diagram of a power MOSFET in parallel with a Schottky diode, as is known in the prior art.

[0024] FIGS. **4A-4E** are schematic top views illustrating five cell geometries that may be used in connection with the merged MOSFET and Schottky diode structures of the present invention.

[0025] **FIG. 5** is a schematic cross-sectional view of a merged MOSFET and Schottky diode structure, in accordance with an embodiment of the present invention. The view in **FIG. 5** is like that taken along line **5--5** in **FIG. 4A** or along line **5--5** in **FIG. 4C**.

[0026] FIGS. **6A-6F** illustrate a process for forming a device like that shown in **FIG. 4**, in accordance with an embodiment of the present invention.

[0027] **FIG. 7** is a schematic cross-section of a merged MOSFET and Schottky diode structure that includes deep p+regions for low resistance contacts to the body regions and to surround the perimeter of the Schottky diode.

[0028] **FIG. 8** is a schematic top view illustrating one cell geometry that may be used in connection with the merged MOSFET and Schottky diode structures of the present invention.

[0029] FIGS. **9A-9D** are schematic top views illustrating various cell geometries that may be used in connection with the merged MOSFET and Schottky diode structures of the present invention.

[0030] **FIG. 10** is a schematic top view illustrating another cell geometry that may be used in connection with the merged MOSFET and Schottky diode structures of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0031] The present invention now will be described more fully hereinafter with reference to the accompanying draw-